THE ALOHA SYSTEM	project: Fast Sync Modem	document no.: CCG/G-76.1	pages: 16 pages
title: ALOHA MODEM MODIFICATIONS		document type: General Document	
		date: January 6, 1976	
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GENERAL

The purpose of this note is to describe design modifications which have been recently implemented in the ALOHA Fast Sync and ATS-1 modem designs. These modifications involve primarily the Noisy Clock Recovery Circuit as well as a change made in the Integrate and Dump Filter circuit. The purpose of the modifications is to improve the ability of the Clock Recovery Circuit to retain synchronization in the presence of signal distortion. It is strongly recommended that these changes be incorporated in any modem using the same circuits as the ALOHA modems for clock recovery and demodulation.

BACKGROUND

Operating experience with the ALOHA network revealed that certain ALOHA terminals tended to receive erroneous packets when certain bit patterns were transmitted to them. These patterns consisted of long strings of ONES with few ZEROES interspersed among them. The errors also tended to occur mainly with terminals using narrow-band radio receivers. Knowing that the Noisy Clock Recovery Circuit could have a phase-ambiguity problem under the condition of all-ONES (no phase reversals), the operation of this circuit under error-prone conditions was studied and found to be the cause of bit-synchronization loss. The phase distortion introduced by the narrow-band receiver increased the probability of missing a zero-crossing in the Noisy

Clock Recovery Circuit. When this happens, this circuit will then lock 180 degrees out of phase until a ZERO (phase reversal) is received to reset the phase reference, or until another zero-crossing is either missed or added. In the Fast Sync and ATS-1 modems, the bandwidth of the loop is relatively large, so that the loop can follow the phase changes of the Noisy Clock Recovery Circuit within a few bit-times. In the TCU modem, the loop has a very narrow bandwidth, so that these phase errors have little effect on the loop's output phase. For this reason, the required design changes have been implemented only in the Fast Sync and ATS-1 modems.

DISCUSSION

A functional diagram of the original Noisy Clock Recovery Circuit is shown in Figure 1. As can be seen, the squaring circuit destroys the phase sense of the biphase signal in the process of deriving the double clock frequency component. Thus this circuit can lock either in phase or 180 degrees out of phase with the incoming data signal. This problem is avoided when sending the ZERO condition, since under this condition the carrier phase is reversed every bit time, resulting in a half-frequency signal which always has zero-crossings at the bit interval boundaries. The circuit includes a 3/4-bit-time inhibit circuit which normally prevents sensing 1/2-bit-time zero-crossings occurring when ONES are received. However, if signal distortion is great enough, this 1/2-bit zero-crossing occurrence may be delayed long enough to not be inhibited and thus introduce an extra erroneous pulse to the frequency divider. Alternatively, the distortion can cause a proper zero-crossing to occur early enough to be inhibited, thus deleting a correct pulse to the frequency divider. Either phenomenon can result in an instantaneous 180

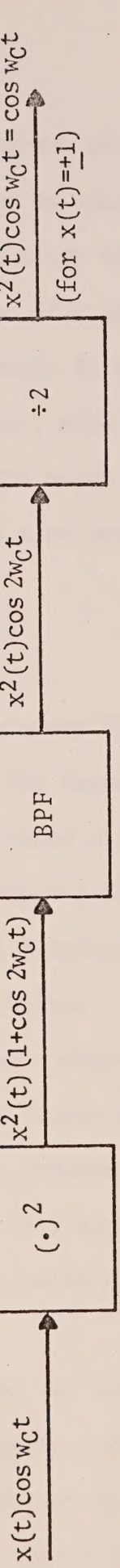

Figure 1

ORIGINAL NOISY CLOCK RECOVERY CIRCUIT

degree phase shift at the output of the frequency divider. One can also see that this circuit would also be sensitive to extra zero-crossings introduced by noise. The phase of the noisy clock out of the frequency divider is restored upon the occurrence of a ZERO, so that with normal data patterns the noisy clock will not remain in an out-of-phase condition for more than a few bit intervals. However, when strings of ONE bits are received, this condition is not true and the noisy clock may remain out of phase long enough to allow the loop to slew over to the out-of-phase condition.

MODIFICATIONS

The new Noisy Clock Recovery Circuit is shown in Figure 2, at a functional level. The portion within the dashed line is already present in the modem's demodulator circuits. The added blocks are the one-bit delay module and the multiplier, both of which replace the blocks shown in Figure 1. The demodulator's multiplier is the PSK demodulator and the low-pass-filter (LPF) is the Digital Integrate and Dump Filter. The one-bit delay module is necessary to compensate for the one-bit processing delay of the integrate and dump filter. The terms shown in Figure 2 are for the in-phase condition of the loop; i.e., the phase error between the loop clock output and the data signal input is zero. Also, since all signals are digital, and thus amplitude limited, amplitudes are all normalized to constant levels of plus or minus one.

This circuit shows that no frequency doubling is performed on the input signal, so that phase-ambiguity problems are avoided. The data modulation is removed from the input signal by multiplying the input signal with the estimate of the modulating signal derived in the demodulator. As shown in

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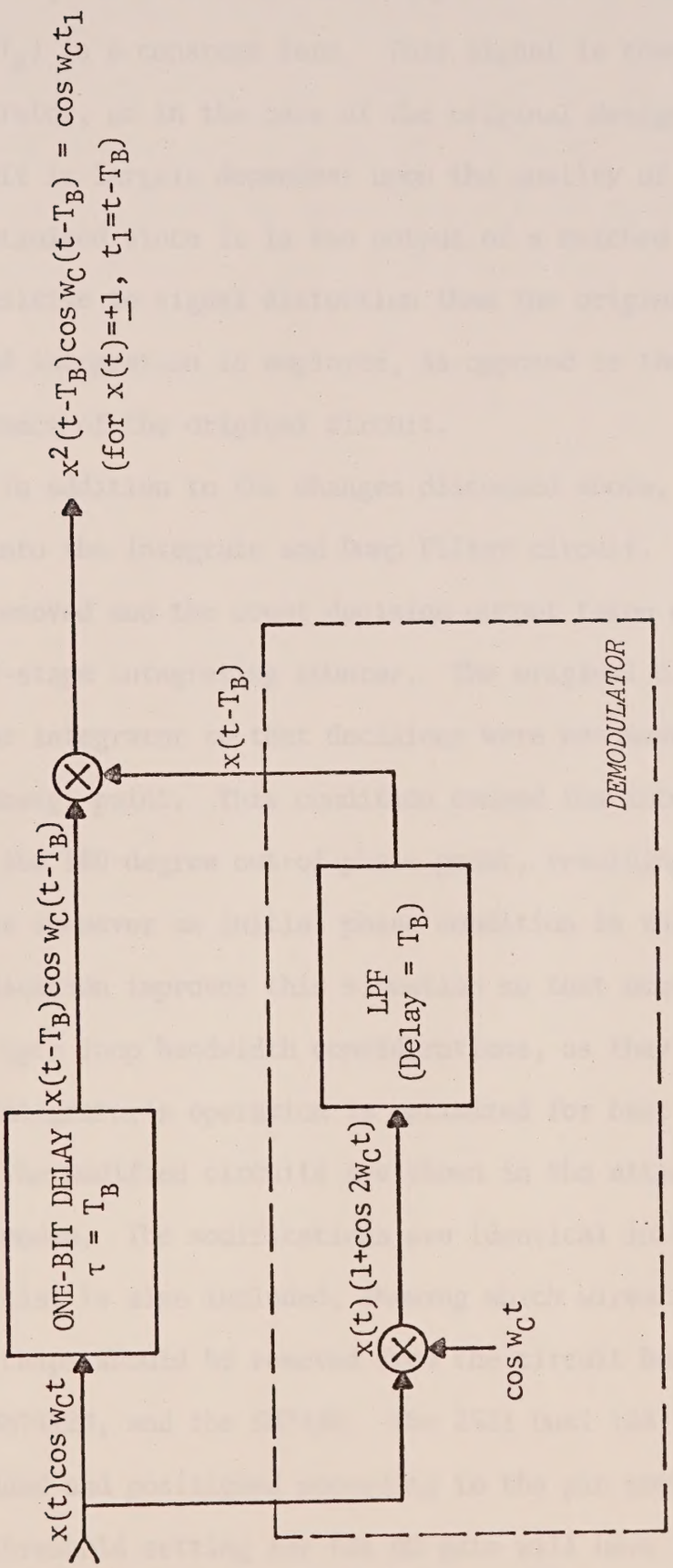


Figure 2

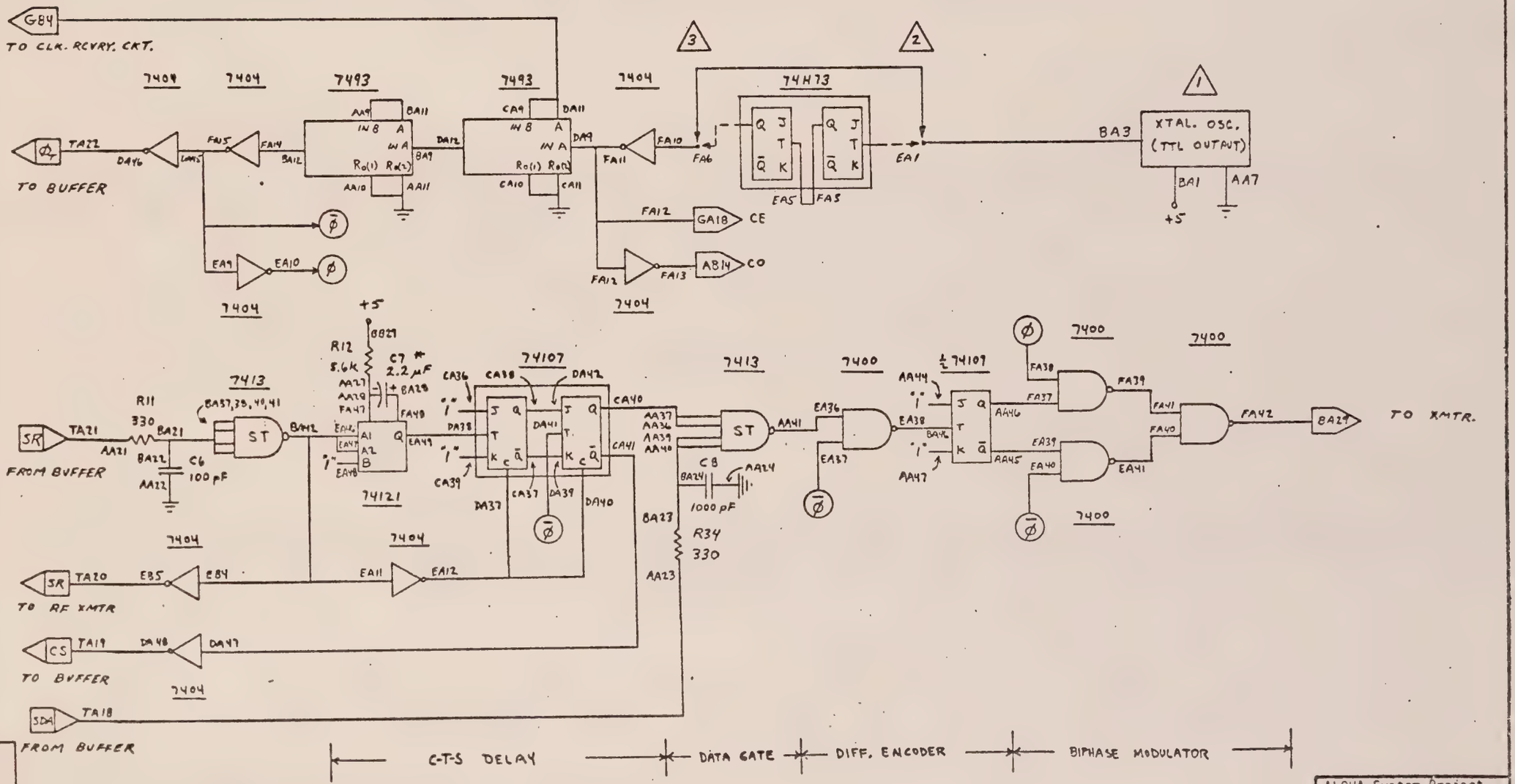
NEW NOISY CLOCK RECOVERY CIRCUIT

Figure 2, the result of the multiplication is the clock frequency only, since $x^2(t-T_B)$ is a constant term. This signal is then fed to the loop's phase comparator, as in the case of the original design. The operation of this circuit is largely dependent upon the quality of the estimate of x(t), which is optimized since it is the output of a matched filter. It is much more insensitive to signal distortion than the original circuit since full bit-period integration is employed, as opposed to the one-fourth bit-period tolerance of the original circuit.

In addition to the changes discussed above, a minor modification was put into the Integrate and Dump Filter circuit. The eight-input decode gate was removed and the count decision output taken off of the last stage of the eight-stage integrating counter. The original circuit introduced a bias in the integrator so that decisions were not made at exactly the one-half bit-energy point. This condition caused the integrator to function improperly near the 180-degree out-of-phase point, resulting in long clock acquisition delays whenever an initial phase condition in this region occurred. The modification improves this situation so that acquisition times are dependent only upon loop bandwidth considerations, as they should be. In addition, the integrator's operation is optimized for best estimates of the data signal.

The modified circuits are shown in the attached drawing of the ALOHA Fast Sync modem. The modifications are identical in the ALOHA ATS-1 modem. A wire list is also included, showing which wires are to be removed and added. Four chips should be removed from the circuit board. These are the two SN74121's, the SN74123, and the SN7430. The 2521 Dual 128-Bit Shift Register chip should be added and positioned according to the pin numbers shown on the drawing. The threshold setting for the RG gate will have to be reset since the average

output of S/N Threshold Detector's integrator will be higher under noise-only conditions due to the circuit changes. This setting should be done with receiver front-end noise only into the modem. The S/N Threshold Adjust potentiometer should be turned until the RG output occurs infrequently (about once every 100 seconds for a false-alarm rate of 10^{-6}).



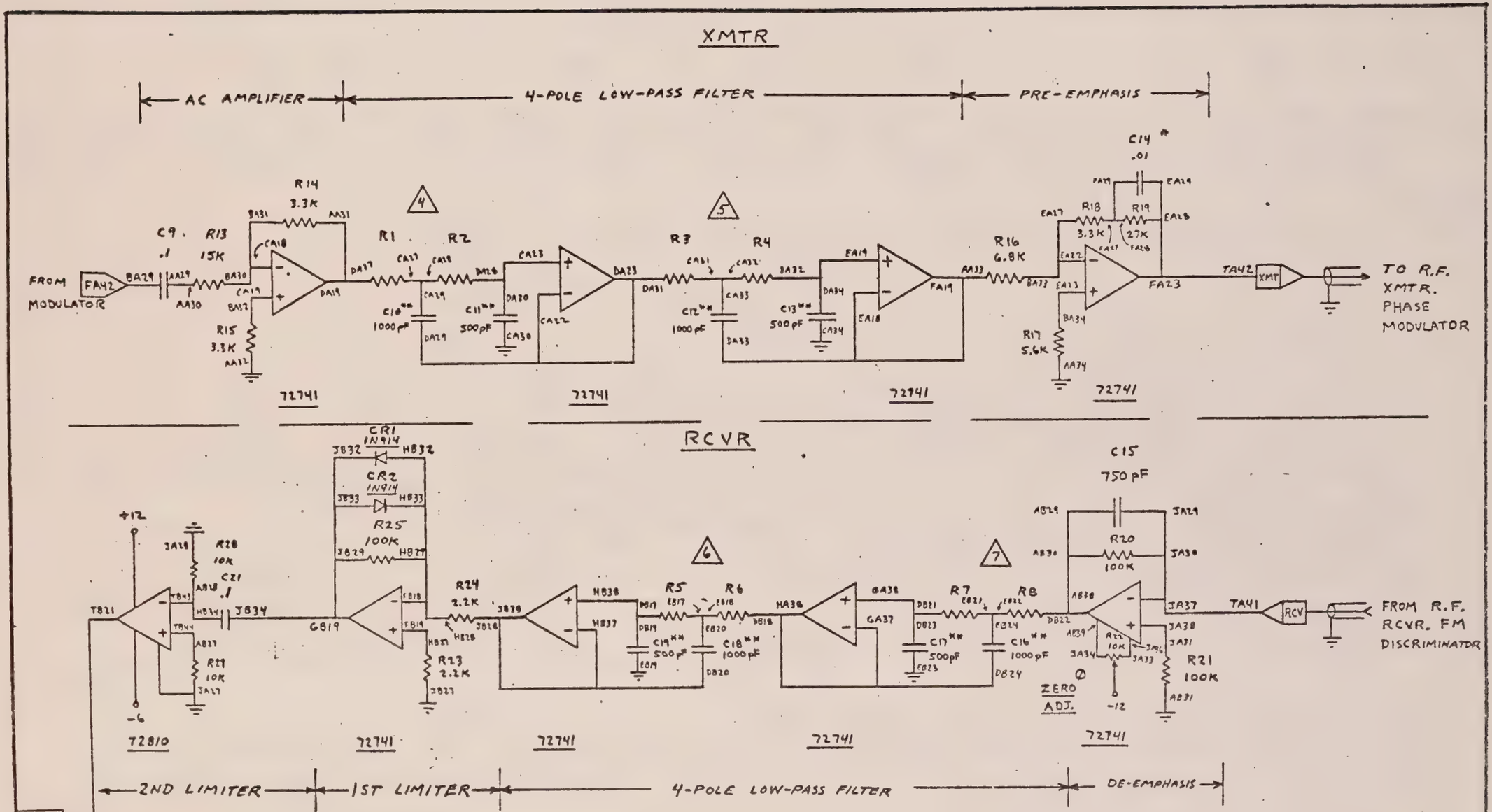
△ — SEE DATA RATE OPTION TABLE

* — 10 % TOLERANCE

RF 1015 - 01

RF1015 -01

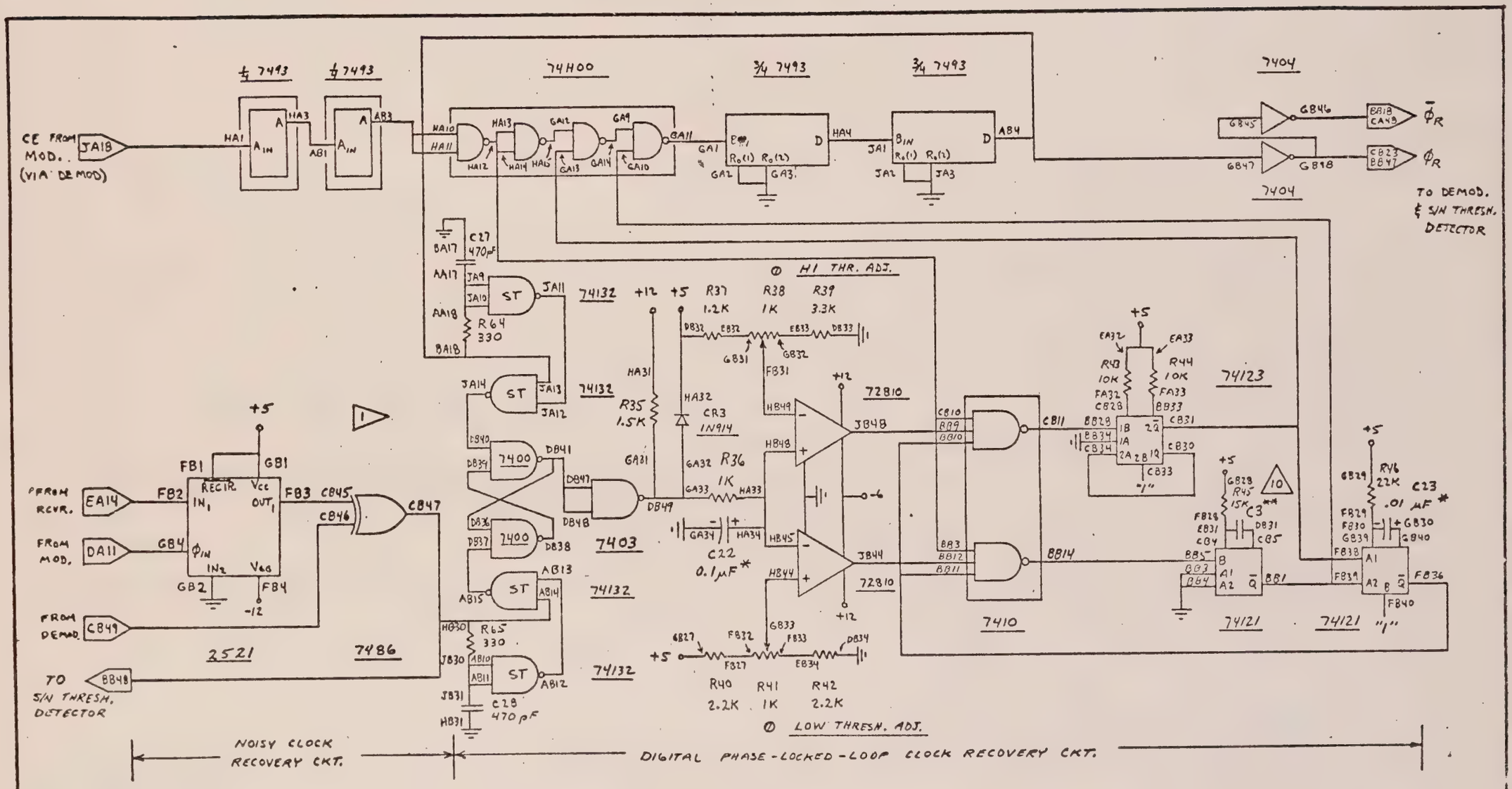
ALOHA System Project,
U. of H.
System: FAST SYNC MODEM
Sub-system: MODULATOR
Name D. Wax
Date 9-10-73
Page 1 of 7



RF1015-02

RF1015-02

ALOHA System Project,
U. of H.
System: FAST SYNC MODEM
Sub-system: XMTR-RCVR
Name D. Wax
Date 9-10-73
Page 2 of 7



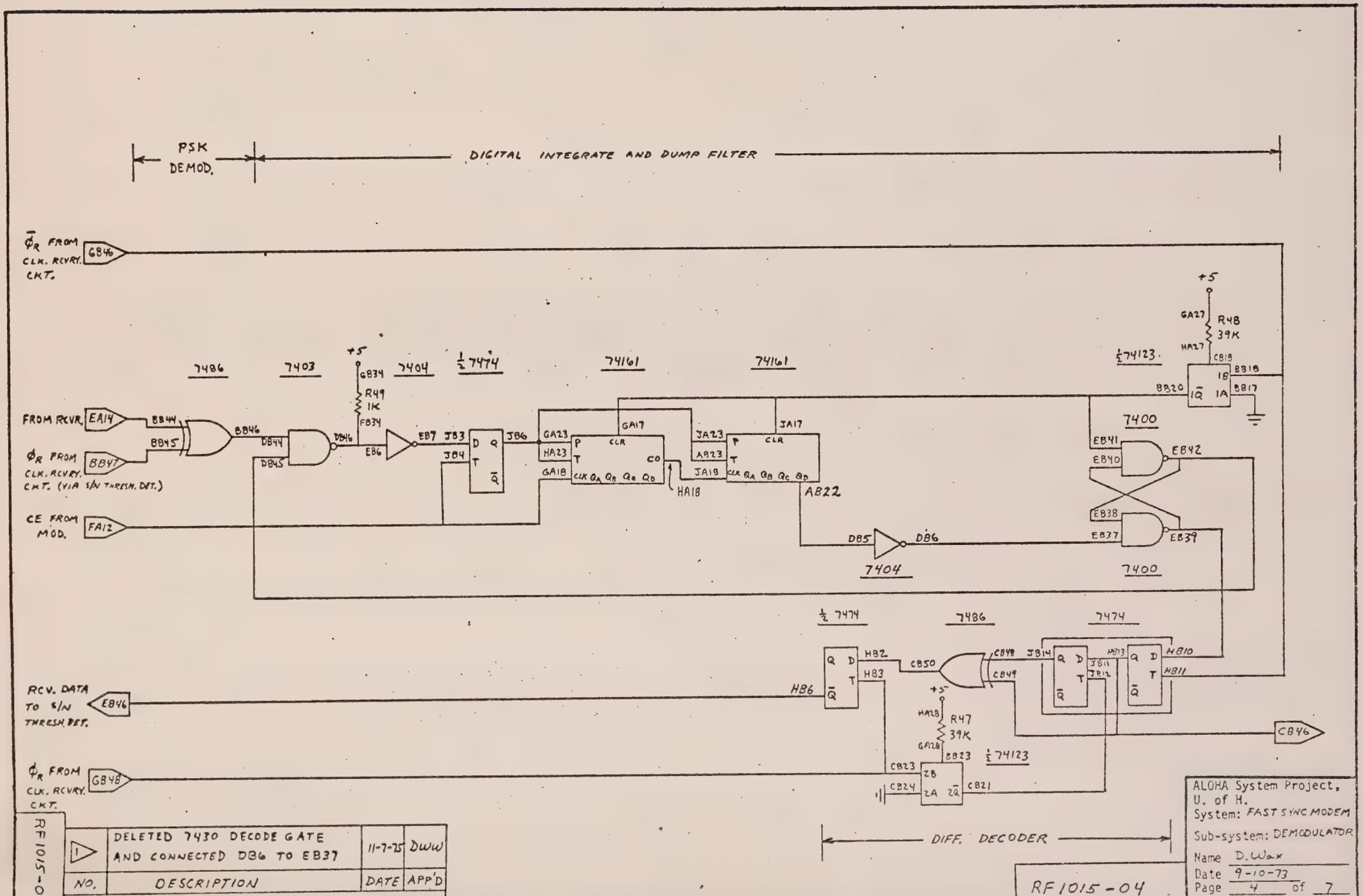
NO.	DESCRIPTION	DATE	APP'D.
1	CHANGED NOISY CLOCK RECOVERY CIRCUIT TO CONFIGURATION SHOWN.	11-7-75	DWW

REVISIONS

RF 1015-03

RF 1015-03

ALOHA System Project,
U. of H.
System: FAST SYNC MODEM
Sub-system: CLOCK RCVRY.
Name D. Wax
Date 9-10-73
Page 3 of 7



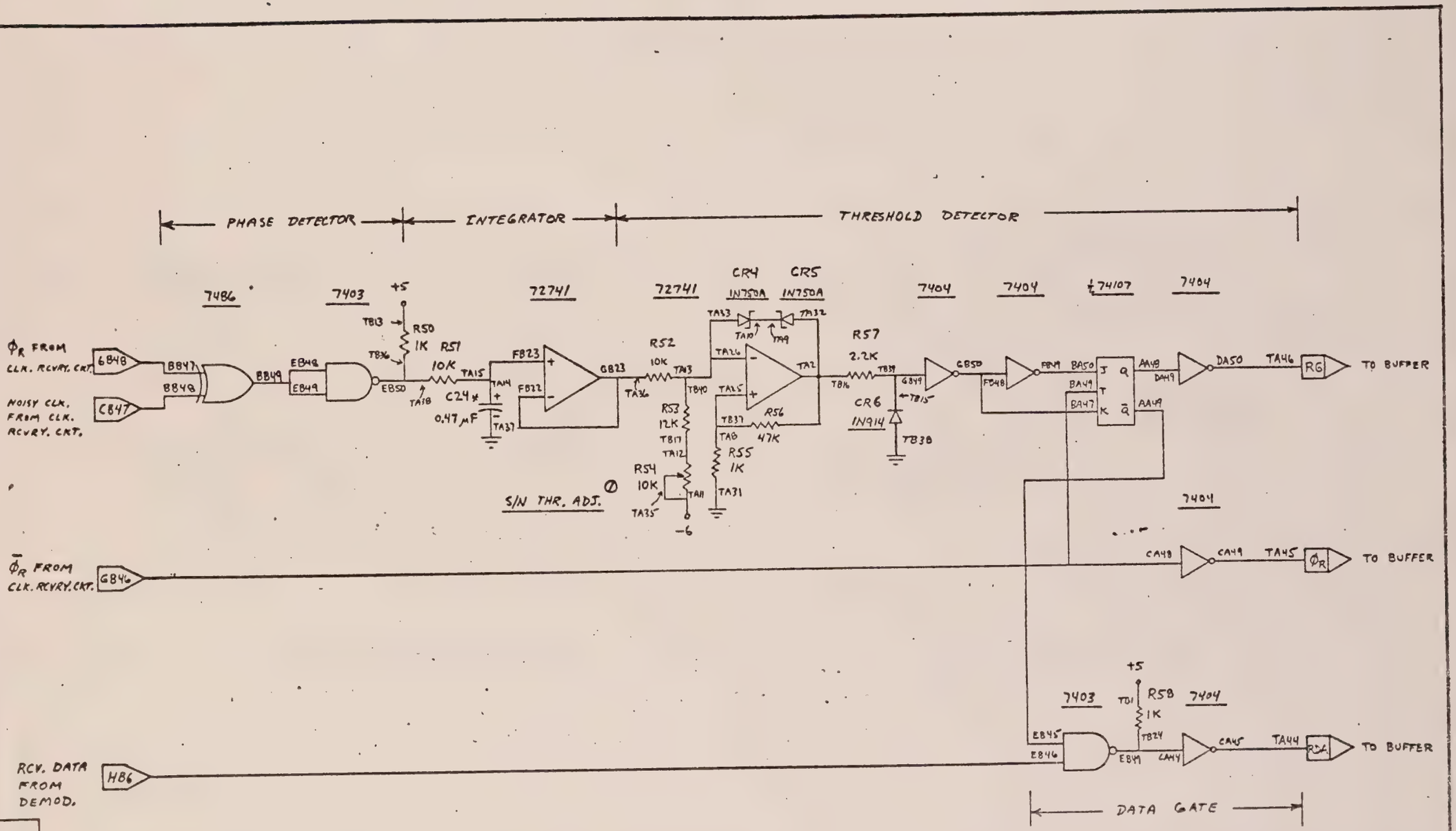
NO.	DESCRIPTION	DATE	APP'D
1	DELETED 7430 DECODE GATE AND CONNECTED DB6 TO EB37	11-7-75	DWW

REVISIONS

RF1015-04

ALOHA System Project, U. of H.
System: FAST SYNC MODEM
Sub-system: DEMODULATOR
Name D. Wax
Date 9-10-73
Page 4 of 7

RF1015-04

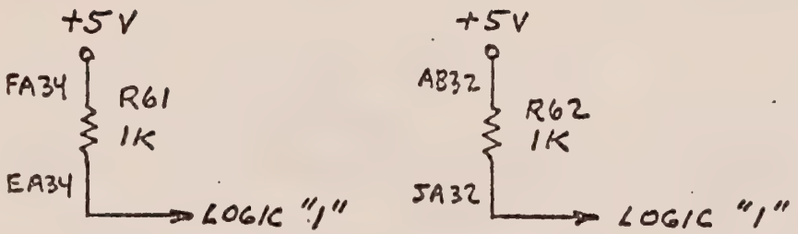


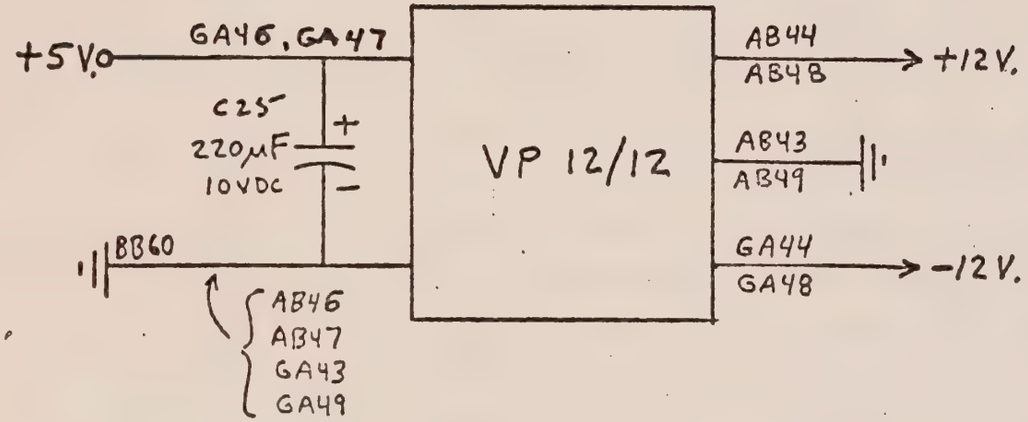
* — 10% TOLERANCE

RF1015-05

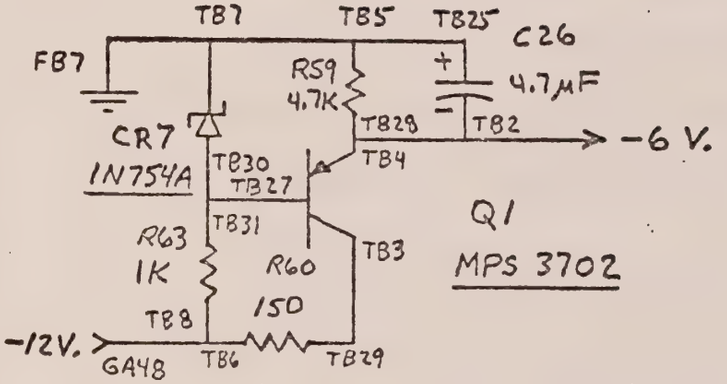
RF1015-05

ALOHA System Project, U. of H.
System: FAST SYNC MODEM
Sub-system: S/N THRESHOLD DETECTOR
Name D. Wax
Date 9-10-73
Page 5 of 7





±12 VOLT SUPPLY



-6 VOLT SUPPLY

RF1015-06

RF1015-06

DATA RATE OPTION TABLE

SYMBOL	PARAMETER	9.6 KBS	24 KBS	UNIT
△1	FREQUENCY	9.8304	6.1440	MHz
(3) △2	JUMPER PIN NO.	NONE	EA1	—
(3) △3	JUMPER PIN NO.	NONE	FA6	—
△4	R1, R2	10K	4.7K	OHMS
△5	R3, R4	10K	4.7K	OHMS
△6	R5, R6	10K	4.7K	OHMS
△7	R7, R8	10K	4.7K	OHMS
△1				
△1				
△10	C3	250	100	pF

NOTES:

(1) ALL RESISTORS ARE $\frac{1}{4}$ WATT, 5% TOLERANCE

(2) CAPACITORS NOTED WITH
* ARE 10% TOLERANCE
** ARE 5% TOLERANCE

(3) FOR 24KBS DATA RATE, REPLACE 74H73 WITH JUMPER PLUG

NO.	DESCRIPTION	DATE	APP'D.
△1	DELETED C1 AND C2	11-7-75	DWW

REVISIONS

RF1015-07

RF1015-07

ORIGIN	FROM PIN	✓	TO PIN	COMMENTS Removals
	EA14		HB17	REMOVE
	HB17		BB44	
	HB17		JB23	
	HB18			→ cut at FB5
	JB27		JB24	
	JB24		GND	
	JB21		FB4	
	HB20		FB3	
	HB23		EA30	
	JB18		EA31	
	FB5			→ cut at FB40
	FB6		FB13	
	FB12		GND	
	FB11		FB12	
	GB4		HA29	
	GB4		EB27	
	EB28		GA30	
	GB12		EB28	
	DB27		GB5	
	DB28		GB13	
	EB30		HA30	
	FA31		VCC	
	FA30		FA31	
	GA29		GA27	
	EB29		VCC	
	DB32		DB29	
	DB29		VCC	
	FB14		BB48	
	HB30		AB14	
	FB14		AB14	
	HA19		DB14	
	HA20		DB13	
	HA21		DB12	
	HA22		DB11	
	AB19		DB10	
	AB20		DB9	
	AB21		EB12	
	AB22		DB5	
	DB6		EB11	
	EB15		EB37	

ALOHA System Project, U. of H.
System Fast Sync Modem
Sub-system Wire List - Modification I
Name _____ Page 1 of 2 Date _____

ORIGIN	FROM PIN	✓	TO PIN	COMMENTS Removals (continued)
	GB1		VCC	
	FB7		GND	
				CONNECTIONS
	JB27		GND	Green Wire
	DB32		VCC	Red Wire
	CB47		BB48	
	AB14		CB47	
	DB6		EB37	
	AB22		DB5	Route over top of wires (minimize loading)
	CB49		CB46	
	EA14		BB44	
	FB2		EA14	
	DA11		GB4	
	FB1		GB1	Red Wire
	GB1		VCC	Red Wire
	GB2		GND	Green Wire
	FB4		-12	Orange Wire
	FB3		CB45	
	HB30		AB14	
	GA27		VCC	

ALOHA System Project, U. of H.
System Fast Sync Modem

Sub-system Wire List - Modification I

Name _____ Date _____

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